WHAT IS CLAIMED IS:

1. An interconnect structure comprising

a contact dielectric layer;

an etch stop layer over the contact dielectric layer;

a trench dielectric layer over the etch stop layer; and

an electrically conductive interconnect in (i) a hole through the contact dielectric layer and the etch stop layer, and (ii) a trench in the trench dielectric layer, wherein

the etch stop layer comprises one member selected from a group consisting of an undoped silicon oxide and a doped silicon oxide; and each of the contact dielectric layer and the trench dielectric layer independently comprises the other member of the group.

2. The interconnect structure according to Claim 1, wherein the etch stop layer comprises an undoped silicon oxide, the contact dielectric layer comprises a first doped silicon oxide and the trench dielectric layer independently comprises a second doped silicon oxide.

3. The interconnect structure according to Claim 2, wherein the first and second doped silicon oxides independently further comprise at least one of fluorine, boron and phosphorus.

4. The interconnect structure according to Claim 2, wherein the first and second doped silicon oxides are independently selected from the group consisting of a fluorosilicate glass; a borosilicate glass; a phosphosilicate glass; and a borophosphosilicate glass.

5. The interconnect structure according to Claim 1, wherein the trench in the trench dielectric layer is wider than the hole through the etch stop and contact dielectric layers.

6. The interconnect structure according to Claim 1, further comprising

a substrate; and

a gate structure on the substrate in contact with the contact dielectric layer.

7. The interconnect structure according to Claim 6, wherein the substrate comprises silicon.

8. The interconnect structure according to Claim 6, wherein the gate structure comprises a gate dielectric layer over the substrate, a gate over the gate dielectric layer, a cap dielectric layer over the gate, and spacers adjacent to the gate and the cap dielectric layer.

9. The interconnect structure according to Claim 1, wherein the electrically conductive interconnect comprises a member selected from the group consisting of Al and Cu.

10. The interconnect structure according to Claim 1, wherein a thickness of the etch stop layer is from 100 Å to 1000 Å.

11. A method comprising selectively etching a trench dielectric layer and a contact dielectric layer in a structure comprising the trench dielectric layer, the contact dielectric layer, and an etch stop layer therebetween comprising undoped silicon oxide and having a hole therein, the hole containing a trench dielectric layer material, with an etch gas including $C_2H_2F_4$.

12. A method of forming an interconnect structure, the method comprising

depositing an etch stop layer, containing an undoped silicon oxide, on a contact dielectric layer containing a first oxide comprising silicon;

forming a hole through the etch stop layer;

depositing a trench dielectric layer, containing a second oxide comprising silicon, on the etch stop layer and in the hole through the etch stop layer;

forming a trench in the trench dielectric layer and a hole through the contact dielectric layer by etching the first and second oxides; and

depositing an electrically conductive interconnect in the trench, the hole through the etch stop layer and the hole through the contact dielectric layer.

13. The method according to Claim 12, wherein forming the trench comprises etching the second oxide with a chemistry containing $C_2H_2F_4$.

14. The method according to Claim 13, wherein forming the hole through the etch stop layer comprises etching with a chemistry containing at least one of C_xF_y (where x = 1-6, and y = (2x-2), 2x or (2x+2), but is at least 4) and $C_aH_bF_c$ (where a = 1 or 2, b = 0-2, and c = (2a+2-b)).

15. A method of forming an interconnect structure, the method comprising

forming a trench in a trench dielectric layer;

forming a first hole through an etch stop layer below the trench dielectric layer, the etch stop layer containing an undoped silicon oxide;

forming a second hole through a contact dielectric layer below the first hole in the etch stop layer, the second hole being aligned with the first hole; and

depositing an electrically conductive interconnect in the first hole, the second hole, and the trench.

16. The method according to Claim 15, wherein forming the trench comprises

etching the second oxide with a chemistry containing $C_2H_2F_4$ and stopping at the etch stop layer; or

etching the second oxide for a predetermined etch time with a chemistry containing at least one of C_xF_y (where x = 1-6, and y = (2x-2), 2x or (2x+2), but is at least 4) and $C_aH_bF_c$, (where a = 1 or 2, b = 0-2, and c = (2a+2-b)).

17. The method according to Claim 16, wherein forming the trench comprises etching with a chemistry containing $C_2H_2F_4$.